REMARKS

Claims 1, 4-7, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung (U.S. Publication Number 2002/0019113). Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung. Claims 2, 3 and 12-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung in view of a conventional method described in FIGs. 1A and 1B of Chung. In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention of claims 1-11, a method of trench isolation includes etching a nitride layer, a first conductive layer and an oxide layer to form a nitride layer pattern, a first conductive layer pattern and an oxide layer pattern. The method further includes etching a portion of a substrate adjacent to the first conductive layer pattern using the nitride layer pattern as a mask to form a trench in the substrate.

Claim 1 is amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the method of trench isolation includes etching a portion of the substrate adjacent to the first conductive layer pattern using the nitride layer pattern as a mask to form the trench in the substrate. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 12-21, a method for manufacturing a non-volatile memory device includes etching a nitride layer, a first conductive layer and a first oxide layer to form a nitride layer pattern, a first conductive layer pattern and an oxide layer pattern. The method further includes etching a portion of a substrate adjacent to the first conductive layer pattern using the nitride layer pattern as a mask to form a trench in the substrate.

Chung discloses, in FIG. 3C, a mask pattern 108 on the nitride layer 105 is used as an etch mask during the etching of the upper portion of the substrate 100 adjacent to the first conductive layer pattern 104 to form trench 109. Chung further discloses a conventional method in FIG. 1B in which a photolithography process is preformed to pattern the nitride layer 15, a first polysilicon layer 13 and a oxide layer 11; thereafter, exposed portions of a substrate 10 are etched

to form trenches 18; and that active regions and floating gates are simultaneously formed during the trench forming process using a single mask.

Chung fails to teach or suggest a method of trench isolation that includes etching a portion of a substrate adjacent to a first conductive layer pattern using a nitride layer pattern as a mask to form a trench in the substrate as claimed in claims 1-11. Instead, in FIG. 3C of Chung, the mask pattern 108 is used as an etch mask to form the trench 109.

Chung fails to teach or suggest the elements of the invention set forth in claims 1-11. Specifically, Chung fails to teach or suggest a method of trench isolation that includes etching a portion of a substrate adjacent to a first conductive layer pattern using a nitride layer pattern as a mask to form a trench in the substrate as claimed in claims 1-11. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1, 4-7, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Chung and claims 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over Chung, is respectfully requested.

Chung further fails to teach or suggest a method for manufacturing a non-volatile memory device that includes etching a portion of a substrate adjacent to a first conductive layer pattern using a nitride layer pattern as a mask to form a trench in the substrate, as claimed in claims 12-21. Although Chung in FIG. 1B discloses that the active regions and floating gates are simultaneously formed during the trench forming process using a single mask, Chung does not specifically disclose that the nitride layer 15 is used as the single mask.

Chung fails to teach or suggest the elements of the invention set forth in claims 1-11 and 12-21. Specifically, Chung fails to teach or suggest a method of trench isolation that includes etching a portion of a substrate adjacent to a first conductive layer pattern using a nitride layer pattern as a mask to form a trench in the substrate as claimed in claims 1-11, and a method for manufacturing a non-volatile memory device that includes etching a portion of a substrate adjacent to a first conductive layer pattern using a nitride layer pattern as a mask to form a trench in the substrate, as claimed in claims 12-21. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 2, 3 and 12-21 under 35 U.S.C. 103(a) as being unpatentable over Chung in view of conventional method

described in FIGs. 1A and 1B of Chung, is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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